ULTRALOW-NOISE, HIGH-PSRR, FAST, RF, 1.5-A LOW-DROPOUT LINEAR REGULATORS

FEATURES

- **1.5-A Low-Dropout Regulator With Enable**
- **Available in Fixed and Adjustable (1.2-V to 5.5-V) Output Versions**
- **High PSRR (49 dB at 10 kHz)**
- **Ultralow Noise (48 μV_{RMS}, TPS78630)**
- **Fast Start-Up Time (50 μs)**
- **Stable With a 1-μF Ceramic Capacitor**
- **Excellent Load/Line Transient Response**
- **Very Low Dropout Voltage (390 mV at Full Load, TPS78630)**
- **6-Pin SOT223 and 5-Pin DDPAK Package**

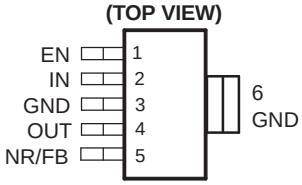
APPLICATIONS

- **RF: VCOs, Receivers, ADCs**
- **Audio**
- **Bluetooth®, Wireless LAN**
- **Cellular and Cordless Telephones**
- **Handheld Organizers, PDAs**

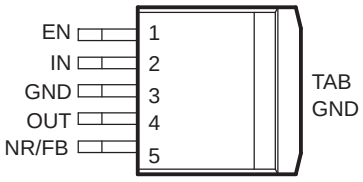
DESCRIPTION

The TPS786xx family of low-dropout (LDO) low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in small outline, SOT223-6 and DDPAK-5 packages. Each device in the family is stable, with a small 1-μF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 390 mV at 1.5 A). Each device achieves fast start-up times (approximately 50 μs with a 0.001 μF bypass capacitor) while consuming very low quiescent current (265 μA, typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA. The TPS78630 exhibits approximately 48 μV_{RMS} of output voltage at 3.0 V output noise with a 0.1 μF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR, low noise features, and the fast response time.

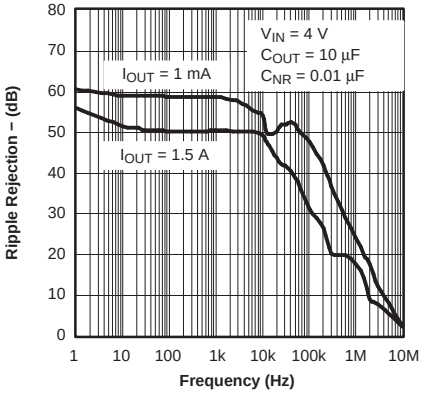
DCQ PACKAGE
SOT223-6
(TOP VIEW)



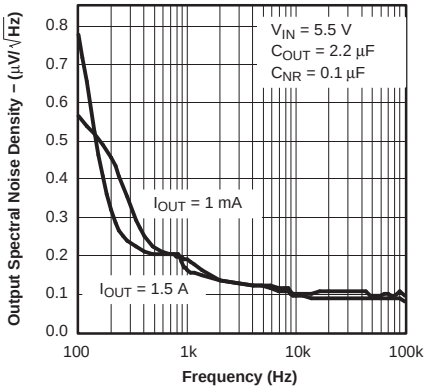
KTT PACKAGE
DDPAK-5
(TOP VIEW)



TPS78630
RIPPLE REJECTION
vs
FREQUENCY



TPS78630
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS786**xxyyyz**	**XX** is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Output voltages from 1.3 V to 5.0 V in 100 mV increments are available; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

Over operating temperature (unless otherwise noted)(1)

	VALUE
V_{IN} range	–0.3 V to 6 V
V_{EN} range	–0.3 V to V_{IN} + 0.3 V
V_{OUT} range	6 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Package Dissipation Ratings table
Junction temperature range, T_J	–40°C to +150°C
Storage temperature range, T_{stg}	–65°C to +150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	BOARD	$R\theta_{JC}$	$R\theta_{JA}$
DDPAK	High-K(1)	2 °C/W	23 °C/W
SOT223	Low-K(2)	15 °C/W	53 °C/W

(1) The JEDEC high-K (2s2p) board design used to derive this data was a 3-in x 3-in (7,5-cm x 7,5-cm), multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.
(2) The JEDEC low-K (1s) board design used to derive this data was a 3-in x 3-in (7,5-cm x 7,5cm), two-layered board with 2 ounce copper traces on top of the board.

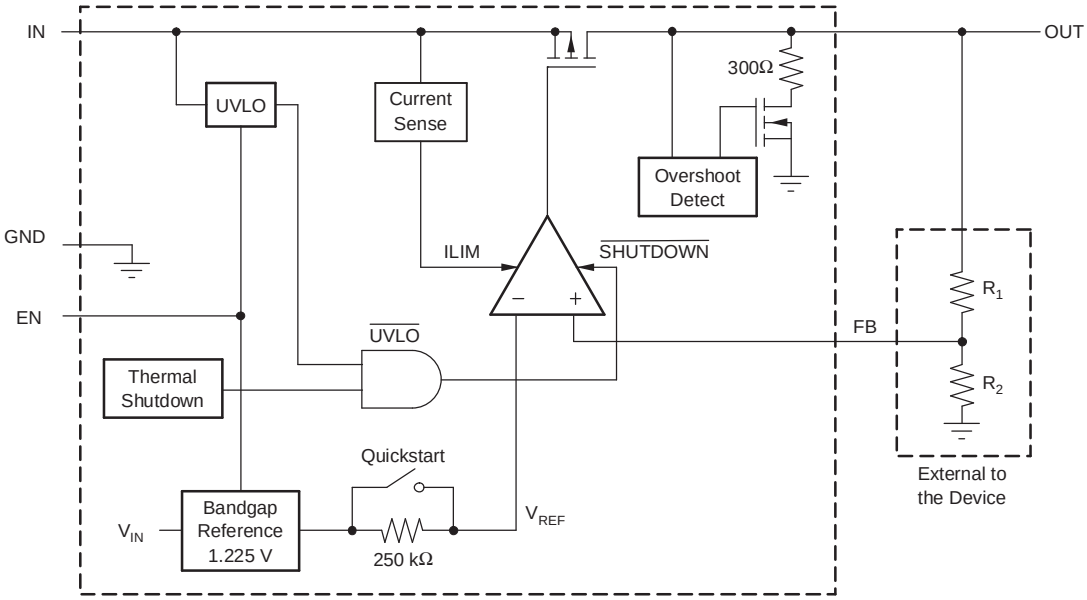
ELECTRICAL CHARACTERISTICS

Over recommended operating temperature range (T_J = –40°C to +125°C), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V(1), I_{OUT} = 1 mA, C_{OUT} = 10 µF, and C_{NR} = 0.01 µF, unless otherwise noted. Typical values are at +25°C.

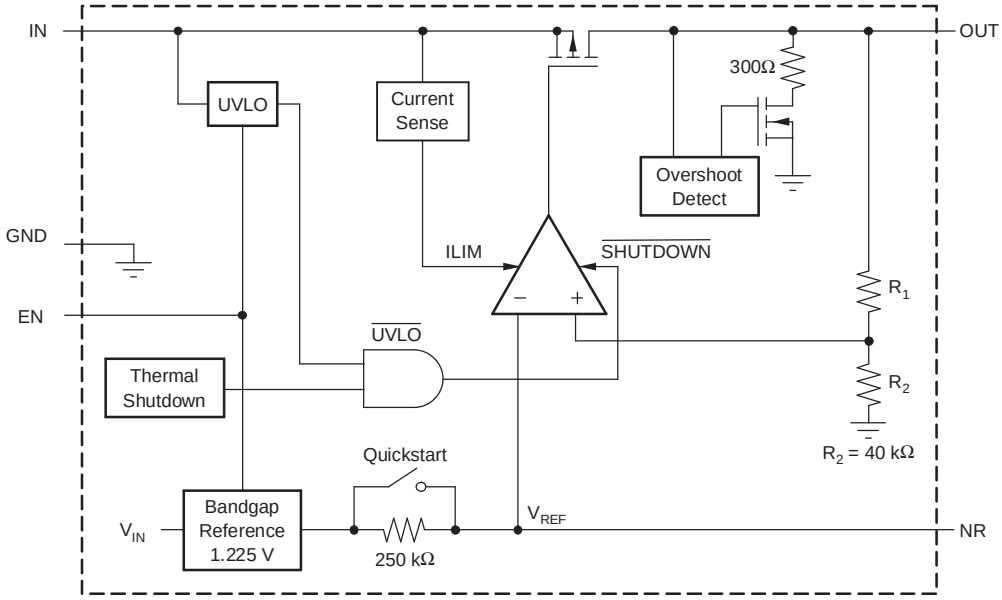
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage, V_{IN} (1)					2.7		5.5	V
Internal reference, V_{FB} (TPS78601)					1.200	1.225	1.250	V
Continuous output current I_{OUT}					0		1.5	A
Output voltage	Output voltage range	TPS78601			1.225		$5.5 – V_{DO}$	V
	Accuracy	TPS78601(2)	0 µA ≤ I_{OUT} ≤ 1.5 A, V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V(1)		$(0.98)V_{OUT}$	V_{OUT}	$(1.02)V_{OUT}$	V
		Fixed V_{OUT} < 5 V	0 µA ≤ I_{OUT} ≤ 1.5 A, V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V(1)		–2.0		+2.0	%
		Fixed V_{OUT} = 5 V	0 µA ≤ I_{OUT} ≤ 1.5 A, V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V(1)		–3.0		+3.0	%
Output voltage line regulation ($\Delta V_{OUT}\%/V_{IN}$)(1)			V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V			5	12	%/V
Load regulation ($\Delta V_{OUT}\%/V_{OUT}$)			0 µA ≤ I_{OUT} ≤ 1.5 A			7		mV
Dropout voltage(3) $V_{IN} = V_{OUT(nom)} – 0.1$ V		TPS78628	I_{OUT} = 1.5 A			410	580	mV
		TPS78630	I_{OUT} = 1.5 A			390	550	
		TPS78633	I_{OUT} = 1.5 A			340	510	
		TPS78650	I_{OUT} = 1.5 A			310	470	
Output current limit			V_{OUT} = 0 V		2.4		4.2	A
Ground pin current			0 µA ≤ I_{OUT} ≤ 1.5 A			260	385	µA
Shutdown current(4)			V_{EN} = 0 V, 2.7 V ≤ V_{IN} ≤ 5.5 V			0.07	1	µA
FB pin current			V_{FB} = 1.225 V				1	µA
Power-supply ripple rejection		TPS78630	f = 100 Hz, I_{OUT} = 10 mA			59		dB
			f = 100 Hz, I_{OUT} = 1.5 A			52		
			f = 10 kHz, I_{OUT} = 1.5 A			49		
			f = 100 kHz, I_{OUT} = 1.5 A			32		
Output noise voltage (TPS78630)			BW = 100 Hz to 100 kHz, I_{OUT} = 1.5 A	C_{NR} = 0.001 µF		66		μV_{RMS}
				C_{NR} = 0.0047 µF		51		
				C_{NR} = 0.01 µF		49		
				C_{NR} = 0.1 µF		48		
Time, start-up (TPS78630)			R_L = 2 Ω, C_{OUT} = 1 µF	C_{NR} = 0.001 µF		50		µs
				C_{NR} = 0.0047 µF		75		
				C_{NR} = 0.01 µF		110		
High-level enable input voltage			2.7 V ≤ V_{IN} ≤ 5.5 V		1.7		V_{IN}	V
Low-level enable input voltage			2.7 V ≤ V_{IN} ≤ 5.5 V		0		0.7	V
EN pin current			V_{EN} = 0		–1		1	µA
UVLO threshold			V_{CC} rising		2.25		2.65	V
UVLO hysteresis						100		mV

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V, whichever is greater. The TPS78650 is tested at V_{IN} = 5.5 V.
(2) Tolerance of external resistors not included in this specification.
(3) Dropout is not measured for TPS78618 or TPS78625 since minimum V_{IN} = 2.7 V.
(4) For adjustable version, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION



Terminal Functions

TERMINAL			DESCRIPTION
NAME	DCQ (SOT223)	KTT (DDPAK)	
NR	5	5	Noise-reduction pin for fixed versions only. An external bypass capacitor, connected to this terminal, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
EN	1	1	The EN terminal is an input that enables or shuts down the device. When EN is a logic high, the device is enabled. When the device is a logic low, the device is in shutdown mode.
FB	5	5	Feedback input voltage for the adjustable device.
GND	3, 6	3, TAB	Regulator ground
IN	2	2	Input supply
OUT	4	4	Regulator output

TYPICAL CHARACTERISTICS

TPS78630 OUTPUT VOLTAGE vs OUTPUT CURRENT

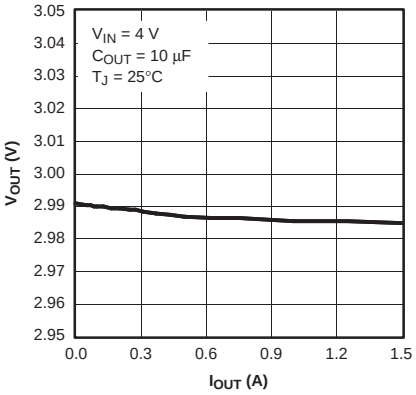


Figure 1.

TPS78628 OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

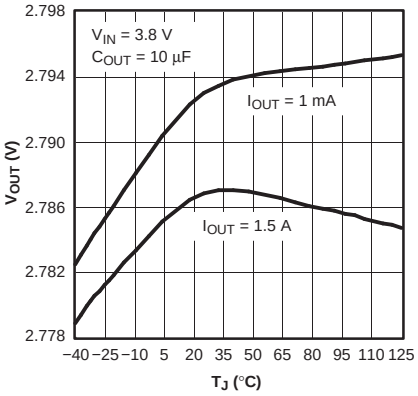


Figure 2.

TPS78628 GROUND CURRENT vs JUNCTION TEMPERATURE

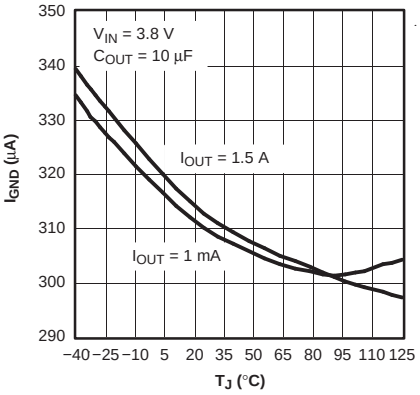


Figure 3.

TPS78630 OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

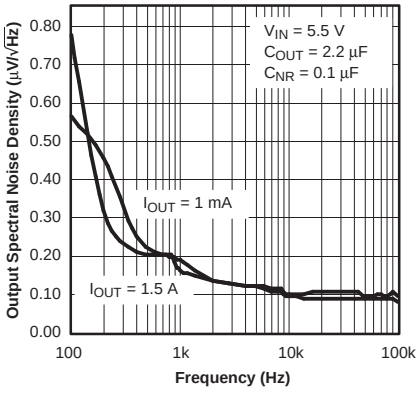


Figure 4.

TPS78630 OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

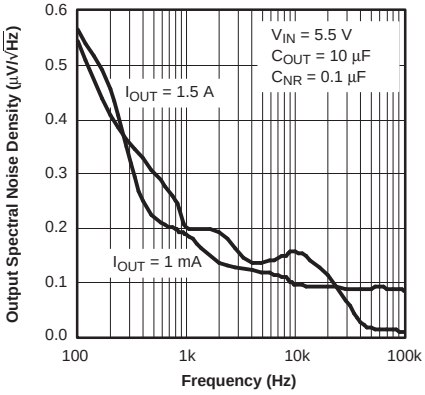


Figure 5.

TPS78630 OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

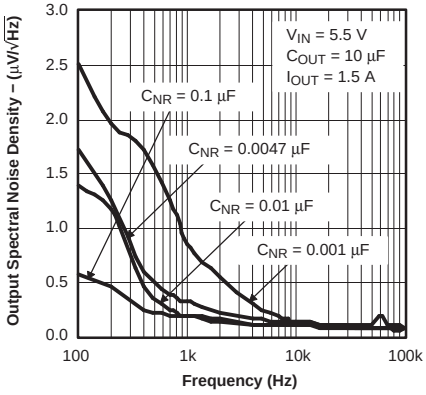


Figure 6.

TPS78630 ROOT MEAN SQUARED OUTPUT NOISE vs BYPASS CAPACITANCE

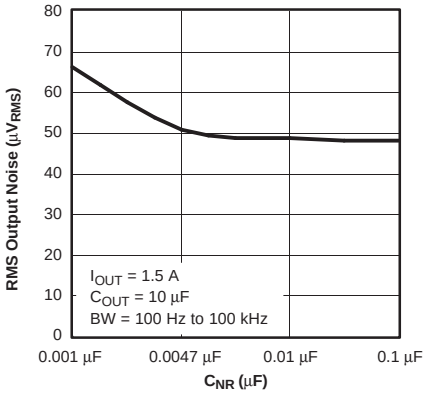


Figure 7.

TPS78628 DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

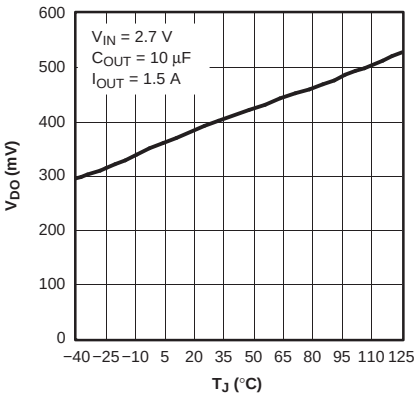


Figure 8.

TPS78630 RIPPLE REJECTION vs FREQUENCY

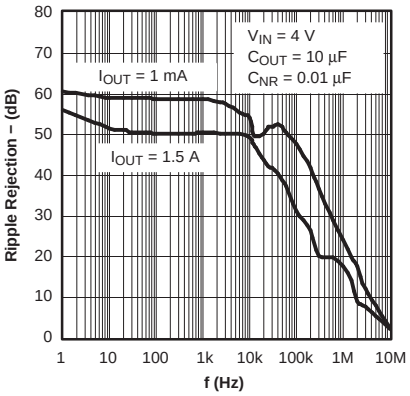


Figure 9.

TYPICAL CHARACTERISTICS (continued)

TPS78630
RIPPLE REJECTION
vs FREQUENCY

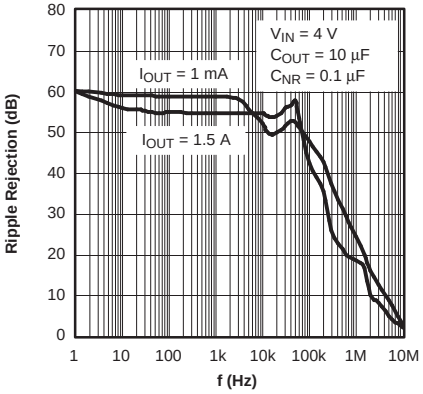


Figure 10.

TPS78630
RIPPLE REJECTION
vs FREQUENCY

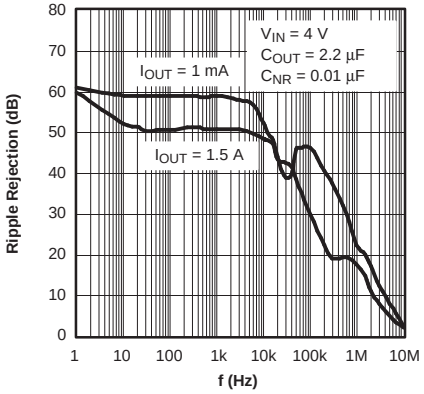


Figure 11.

TPS78630
RIPPLE REJECTION
vs FREQUENCY

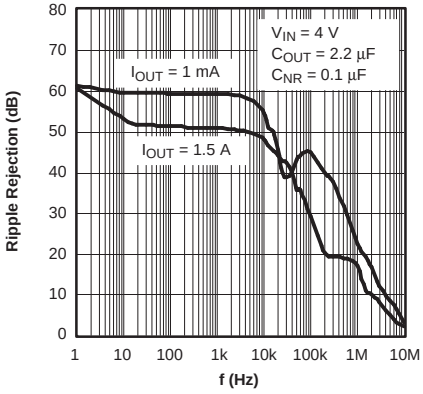


Figure 12.

TPS78618
LINE TRANSIENT RESPONSE

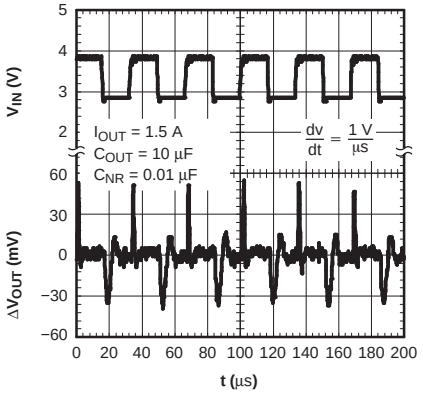


Figure 13.

TPS78630
LINE TRANSIENT RESPONSE

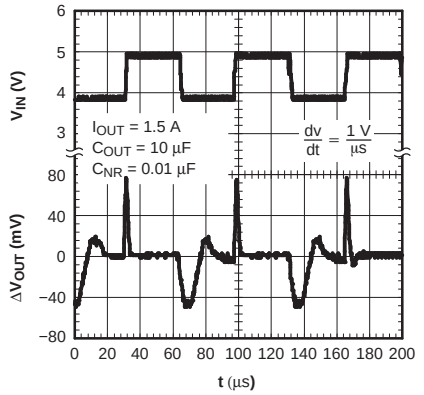


Figure 14.

TPS78628
LOAD TRANSIENT RESPONSE

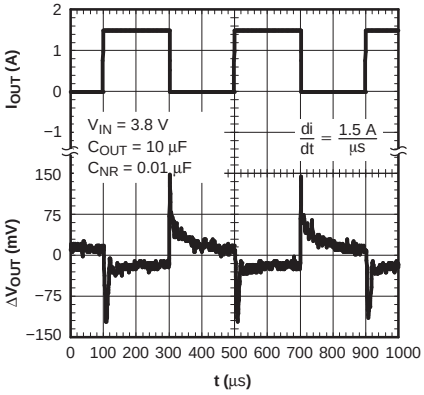


Figure 15.

TPS78625
POWER-UP/
POWER-DOWN

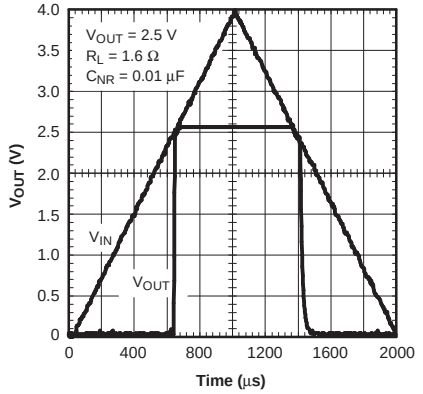


Figure 16.

TPS78630
DROPOUT VOLTAGE
vs OUTPUT CURRENT

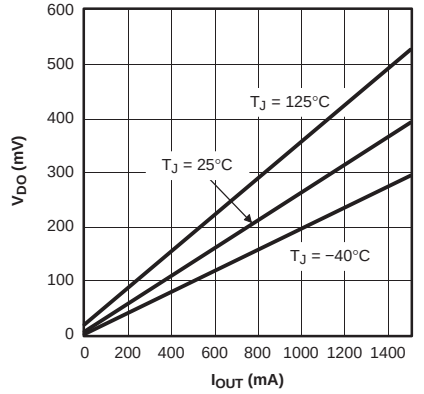


Figure 17.

TPS78601
DROPOUT VOLTAGE
vs INPUT VOLTAGE

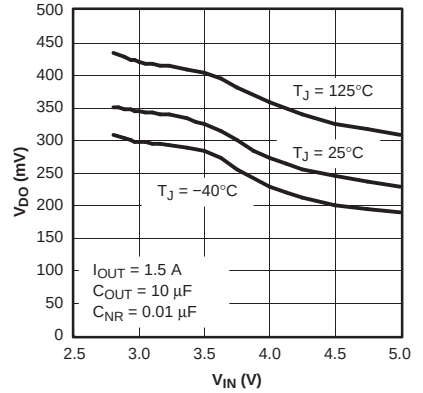


Figure 18.

TYPICAL CHARACTERISTICS (continued)

MINIMUM REQUIRED INPUT VOLTAGE vs OUTPUT VOLTAGE

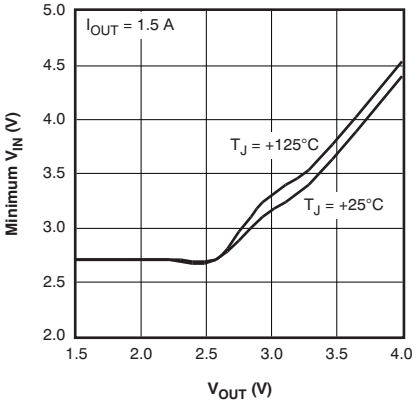


Figure 19.

TPS78630 TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

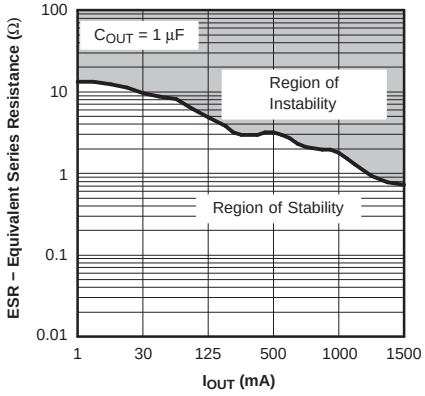


Figure 20.

TPS78630 TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

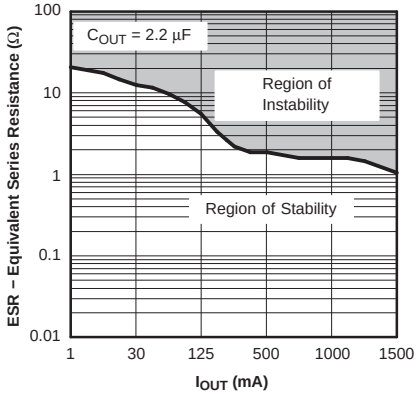


Figure 21.

TPS78630 TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

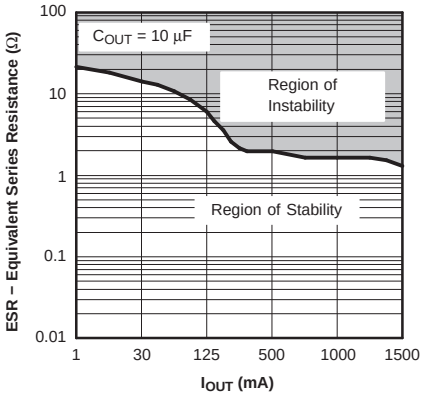


Figure 22.

START-UP

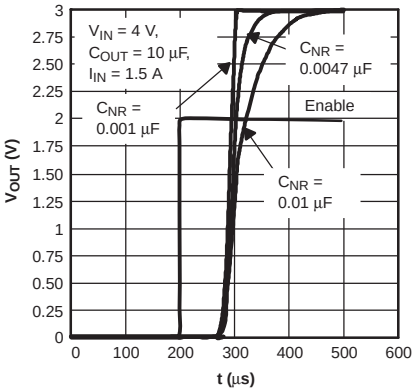


Figure 23.

APPLICATION INFORMATION

The TPS786xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265 μA, typically), and enable input to reduce supply currents to less than 1 μA when the regulator is turned off.

A typical application circuit is shown in Figure 24.

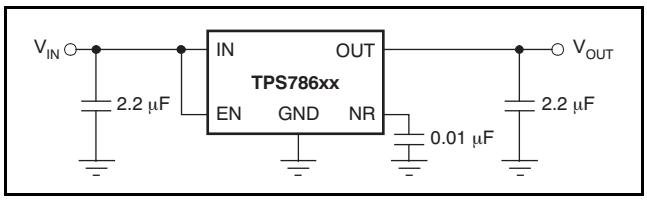


Figure 24. Typical Application Circuit

EXTERNAL CAPACITOR REQUIREMENTS

A 2.2-μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS786xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low-dropout regulators, the TPS786xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1 μF. Any 1 μF or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS786xx has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1-μF to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the functional block diagram.

For example, the TPS78630 exhibits only 48 μV_{RMS} of output voltage noise using a 0.1-μF ceramic bypass capacitor and a 10-μF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

REGULATOR MOUNTING

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in Application Report SBFA015, *Solder Pad Recommendations for Surface-Mount Devices*, available from the TI web site at www.ti.com.

PROGRAMMING THE TPS78601 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS78601 adjustable regulator is programmed using an external resistor divider as shown in Figure 25. The output voltage is calculated using Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where:

- V_{REF} = 1.2246 V typ (the internal reference voltage)

Resistors R_1 and R_2 should be chosen for approximately 40-µA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose R_2 = 30.1 kΩ to set the divider current at 40 µA, C_1 = 15 pF for stability, and then calculate R_1 using Equation 2:

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \quad (2)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB.

The approximate value of this capacitor can be calculated using Equation 3:

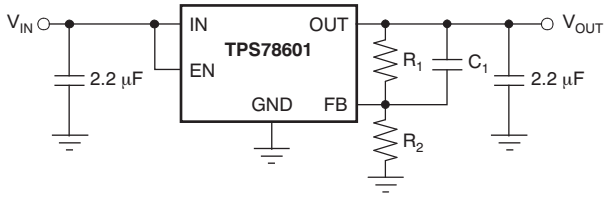
$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2 µF instead of 1 µF.

REGULATOR PROTECTION

The TPS786xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS786xx features internal current limiting and thermal protection. During normal operation, the TPS786xx limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately +165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately +140°C, regulator operation resumes.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	C_1
1.8 V	14.0 kΩ	30.1 kΩ	33 pF
3.6 V	57.9 kΩ	30.1 kΩ	15 pF

Figure 25. TPS78601 Adjustable LDO Regulator Programming

THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature ($T_J$max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ($P_D$max) consumed by a linear regulator is computed as shown in Equation 4:

$$P_D\,max = \left(V_{IN(avg)} - V_{OUT(avg)}\right) \times I_{OUT(avg)} + V_{IN(avg)} \times I_Q \quad (4)$$

where:

- $V_{IN(avg)}$ is the average input voltage.
- $V_{OUT(avg)}$ is the average output voltage.
- $I_{OUT(avg)}$ is the average output current.
- I_Q is the quiescent current.

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{IN(avg)} \times I_Q$ can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\theta JC}$), the case to heatsink ($R_{\theta CS}$), and the heatsink to ambient ($R_{\theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

Figure 26 illustrates these thermal resistances for (a) a SOT223 package mounted in a JEDEC low-K board, and (b) a DDPAK package mounted on a JEDEC high-K board.

Equation 5 summarizes the computation:

$$T_J = T_A + P_D max \times \left(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}\right) \quad (5)$$

The $R_{\theta JC}$ is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator data sheet. The $R_{\theta SA}$ is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks can have $R_{\theta CS}$ values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The $R_{\theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a SOT223 package, $R_{\theta CS}$ of 1°C/W is reasonable.

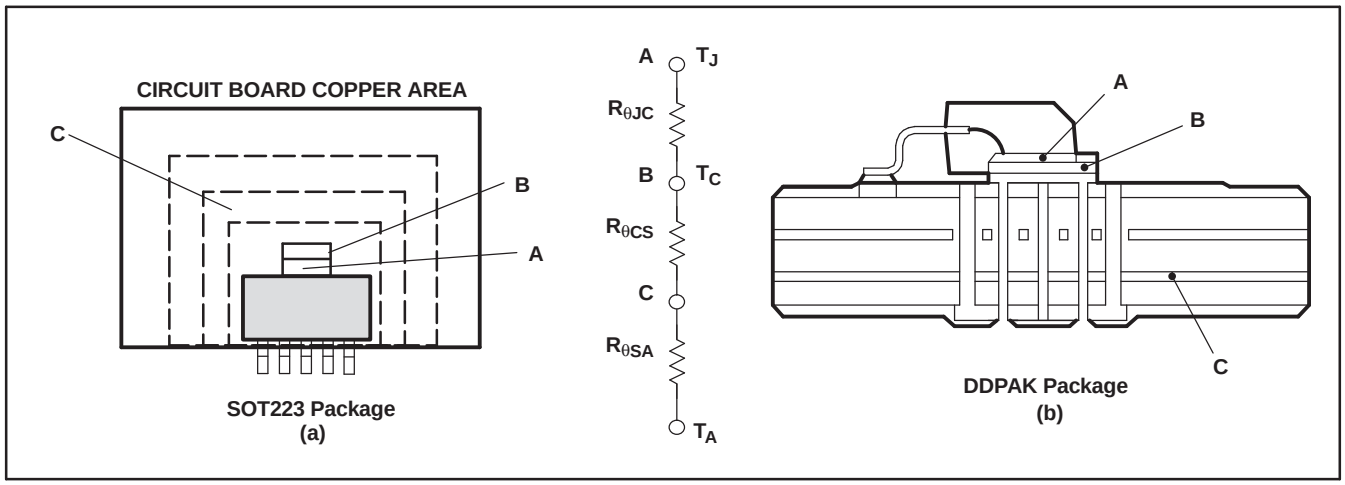


Figure 26. Thermal Resistances

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted provides some heatsinking through the pin solder connections. Some packages, like the DDPAK and SOT223 packages, use a copper plane underneath the package or the circuit board ground plane for additional heatsinking to improve their thermal performance. Computer-aided thermal modeling can be used to compute very accurate approximations of an integrated circuit's thermal performance in different operating environments (for example, different types of circuit boards, different types and sizes of heatsinks, different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ($R_{\theta JA}$). This $R_{\theta JA}$ is valid only for the specific operating environment used in the computer model.

Equation 5 simplifies into Equation 6:

$$T_J = T_A + P_D max \times R_{\theta JA} \quad (6)$$

Rearranging Equation 6 gives Equation 7:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D max} \quad (7)$$

Using Equation 6 and the computer model generated curves shown in Figure 27 and Figure 30, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

DDPAK POWER DISSIPATION

The DDPAK package provides an effective means of managing power dissipation in surface mount applications. The DDPAK package dimensions are provided in the mechanical drawing section at the end of the data sheet. The addition of a copper plane directly underneath the DDPAK package enhances the thermal performance of the package.

To illustrate, the TPS78625 in a DDPAK package was chosen. For this example, the average input voltage is 5 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature +55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is shown in Equation 8:

$$P_D max = (5 - 2.5)\,V \times 1\,A = 2.5\,W \quad (8)$$

Substituting $T_J max$ for T_J into Equation 6 gives Equation 9:

$$R_{\theta JA} max = (125 - 55)°C/2.5\,W = 28°C/W \quad (9)$$

From Figure 27, *DDPAK Thermal Resistance vs Copper Heatsink Area*, the ground plane needs to be 1 cm^2 for the part to dissipate 2.5 W. The operating environment used in the computer model to construct Figure 27 consisted of a standard JEDEC High-K board (2S2P) with a 1 oz. internal copper plane and ground plane. The package is soldered to a 2 oz. copper pad. The pad is tied through thermal vias to the 1 oz. ground plane. Figure 28 shows the side view of the operating environment used in the computer model.

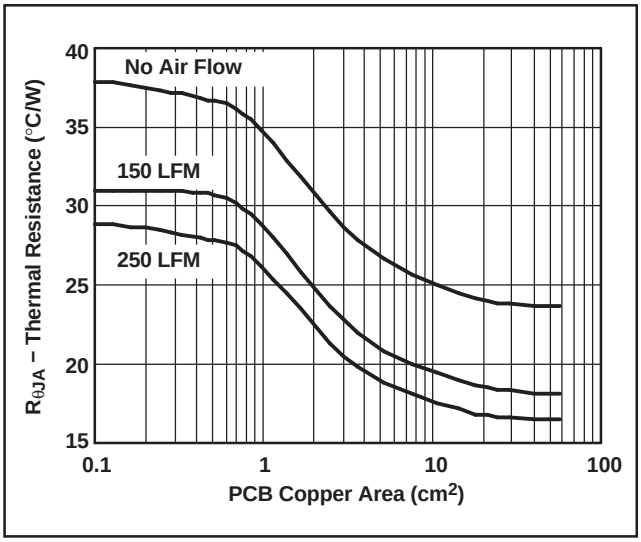


Figure 27. DDPAK Thermal Resistance vs PCB Copper Area

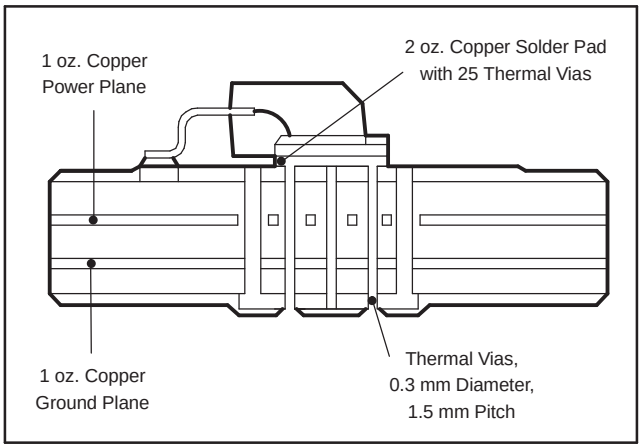


Figure 28. DDPAK Thermal Resistance Computer Model

From the data in Figure 29 and rearranging Equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed.

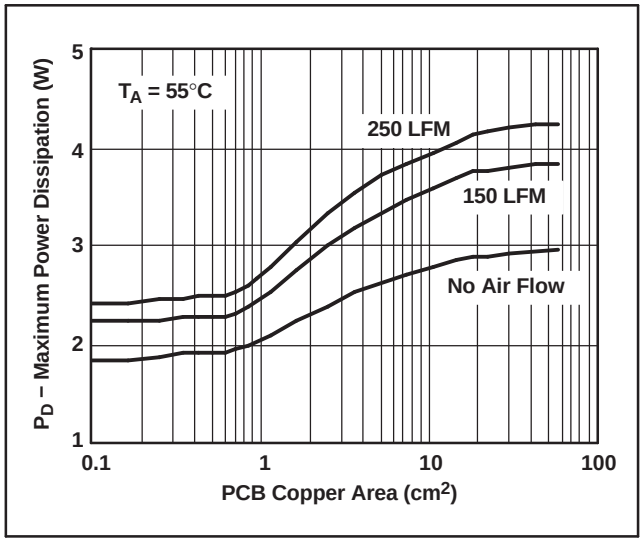


Figure 29. DDPAK Maximum Power Dissipation vs PCB Copper Area

SOT223 POWER DISSIPATION

The SOT223 package provides an effective means of managing power dissipation in surface-mount applications. The SOT223 package dimensions are provided in the mechanical drawing section at the end of the data sheet. The addition of a copper plane directly underneath the SOT223 package enhances the thermal performance of the package.

To illustrate, the TPS78625 in a SOT223 package was chosen. For this example, the average input voltage is 3.3 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature +55°C, no air flow is present, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is calculated as shown in Equation 10:

$$P_D\text{max} = (3.3 - 2.5)\ \text{V} \times 1\ \text{A} = 800\ \text{mW} \quad (10)$$

Substituting $T_J$max for T_J into Equation 6 gives Equation 11:

$$R_{\theta JA}\text{max} = (125 - 55)°\text{C}/800\ \text{mW} = 87.5°\text{C/W} \quad (11)$$

From Figure 30, *$R_{\theta JA}$ vs PCB Copper Area*, the ground plane needs to be 0.55 in^2 for the part to dissipate 800 mW. The operating environment used to construct Figure 30 consisted of a board with 1 oz. copper planes. The package is soldered to a 1 oz. copper pad on the top of the board. The pad is tied through thermal vias to the 1 oz. ground plane.

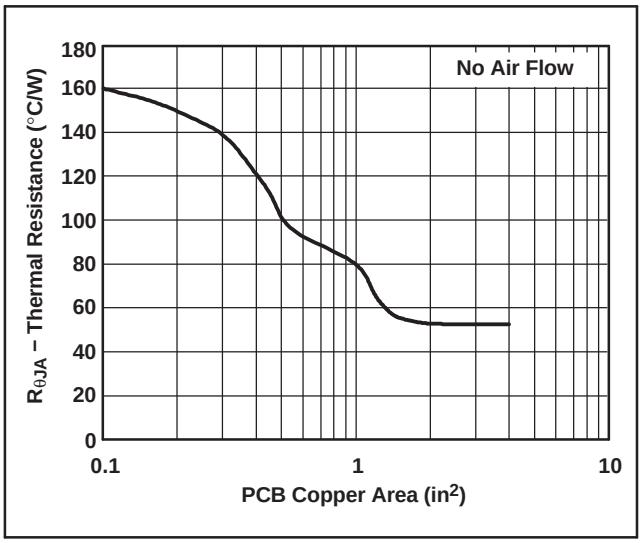


Figure 30. SOT223 Thermal Resistance vs PCB Copper Area

From the data in Figure 30 and rearranging Equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed, as shown in Figure 31.

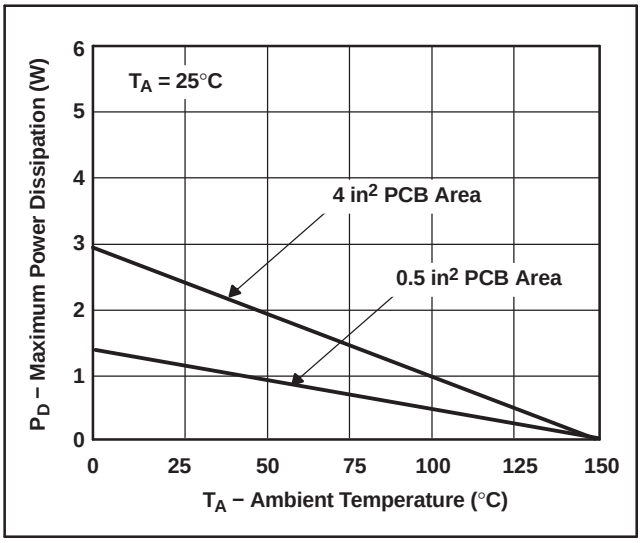


Figure 31. SOT223 Maximum Power Dissipation vs Ambient Temperature

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS78601DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78601DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78601DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78601DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78601KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS78601KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78601KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78601KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78601KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78618DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78618DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78618DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78618DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78618KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS78618KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78618KTTRE3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78618KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78618KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78618KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78625DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78625DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78625DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78625DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78625KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS78625KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS78625KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78625KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78625KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78628DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78628DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78628DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78628DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78628KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS78628KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78628KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78628KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78628KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78630DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78630DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78630DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78630DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78630KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS78630KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78630KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78630KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78630KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78633DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78633DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78633DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78633DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS78633KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS78633KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78633KTTRE3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78633KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78633KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78633KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS78650DCQR	PREVIEW	SOT-223	DCQ	6	2500	TBD	Call TI	Call TI
TPS78650DCQT	PREVIEW	SOT-223	DCQ	6		TBD	Call TI	Call TI

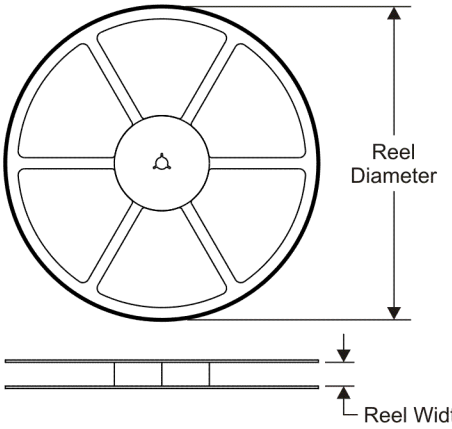
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

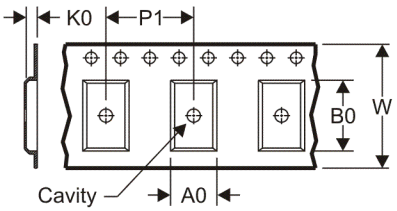
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

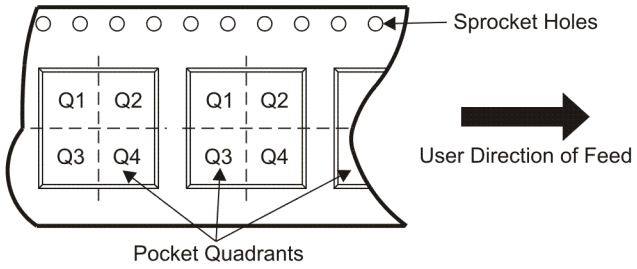


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

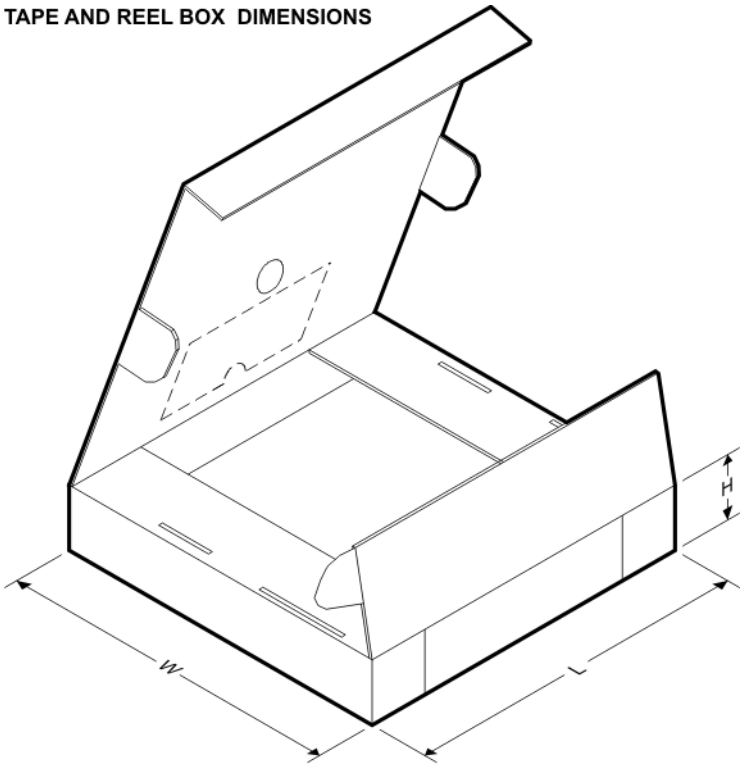


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78601DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS78601KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78601KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78618DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS78618KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78618KTTRE3	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78618KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78625DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS78625KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78625KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78628DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS78628KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78628KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78630DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS78630KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78630KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78633DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS78633KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78633KTTRE3	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS78633KTTT	DDPAK/ TO-263	KTT	5	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

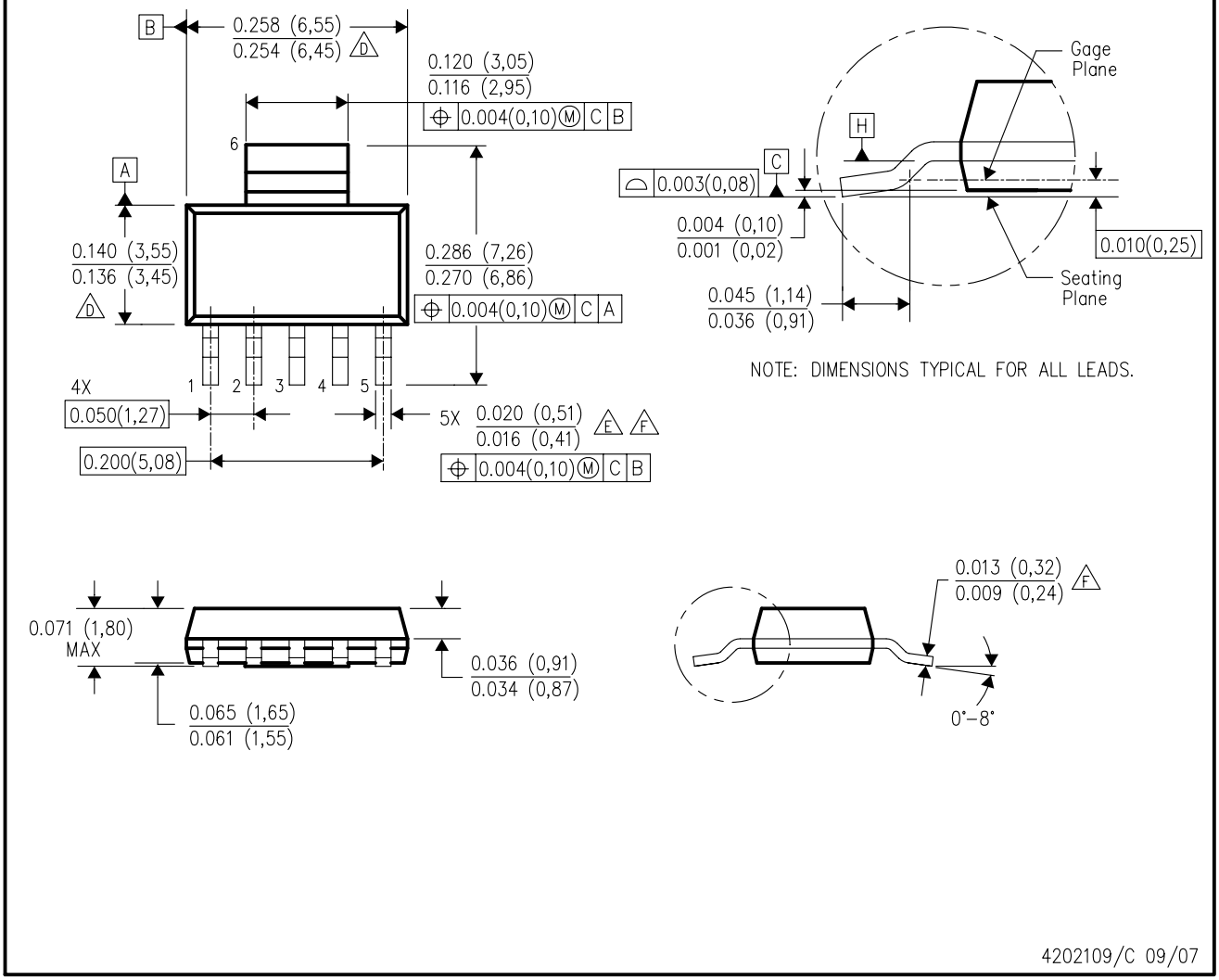


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78601DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS78601KTTR	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS78601KTTT	DDPAK/TO-263	KTT	5	50	346.0	346.0	41.0
TPS78618DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS78618KTTR	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0

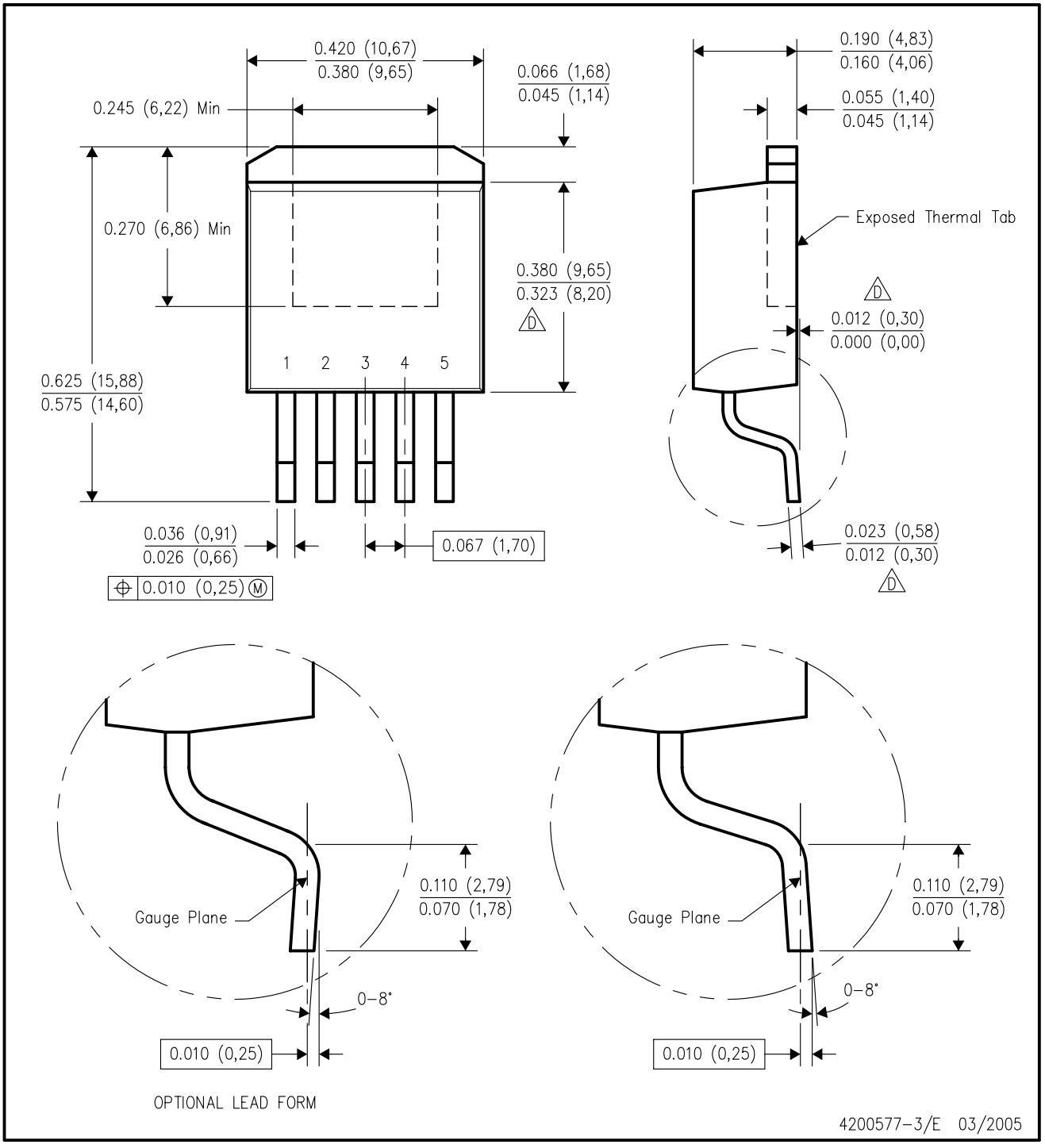
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78618KTTRE3	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS78618KTTT	DDPAK/TO-263	KTT	5	50	346.0	346.0	41.0
TPS78625DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS78625KTTR	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS78625KTTT	DDPAK/TO-263	KTT	5	50	346.0	346.0	41.0
TPS78628DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS78628KTTR	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS78628KTTT	DDPAK/TO-263	KTT	5	50	346.0	346.0	41.0
TPS78630DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS78630KTTR	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS78630KTTT	DDPAK/TO-263	KTT	5	50	346.0	346.0	41.0
TPS78633DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS78633KTTR	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS78633KTTRE3	DDPAK/TO-263	KTT	5	500	346.0	346.0	41.0
TPS78633KTTT	DDPAK/TO-263	KTT	5	50	346.0	346.0	41.0

DCQ (R–PDSO–G6) PLASTIC SMALL–OUTLINE



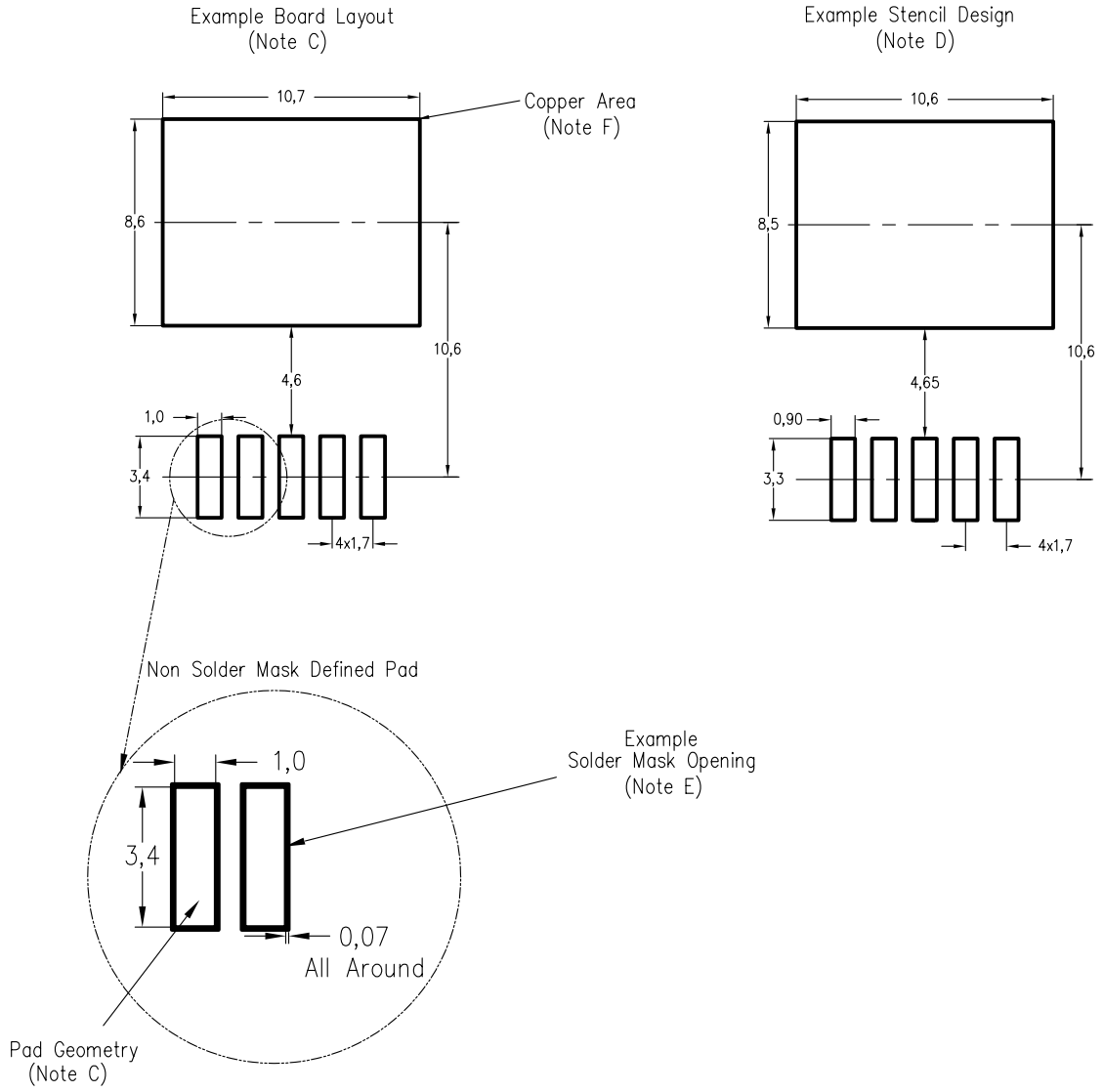
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension in inches.
- D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- E. Lead width dimension does not include dambar protrusion.
- F. Lead width and thickness dimensions apply to solder plated leads.
- G. Interlead flash allow 0.008 inch max.
- H. Gate burr/protrusion max. 0.006 inch.
- I. Datums A and B are to be determined at Datum H.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265